AMENDMENTS TO THE CLAIMS

1. (Cancelled)

2. (Currently amended) ~~Capacitive feedback circuit according to claim 1, further comprising~~ A capacitive feedback circuit, comprising:

a voltage input terminal;

a current output terminal;

a feedback capacitor, having a first terminal connected to input terminal and having a second terminal connected to a high-impedance node;

[[an]] a current amplifying element having a high-impedance control terminal connected to said node;

a current sensor connected in series between said current amplify element and a first supply voltage; and

a bias current source connected in series between said current amplifying element and a second supply voltage.

3. (Original) Capacitive feedback circuit according to claim 2, wherein said current sensor is part of a current-to-voltage converting feedback loop, which has a high-impedance output terminal connected to said node.

4. (Original) Capacitive feedback circuit according to claim 3, wherein the current sensor has an output providing a current output signal, and wherein the feedback loop comprises a comparator, having one current input connected to said current output of the current sensor, having a second input connected to receive a reference current, and having a voltage output connected to said node.

5. (Currently amended) Capacitive feedback circuit according to claim 2, wherein the output terminal is connected to ~~the~~ a node between the current amplifying element and the bias current source.

6. (Currently amended) Capacitive feedback circuit according to claim 2, wherein the output terminal is connected to ~~the~~ a node between the current amplifying element and the current sensor.

7. (Currently amended) Capacitive feedback circuit according to claim ~~2~~ 4, wherein the current amplifying element comprises a first transistor, ~~preferably a MOSFET,~~ having its gate connected to said node.

8. (Currently amended) Capacitive feedback circuit according to claim 2, wherein the bias current source comprises a second transistor, ~~preferably a MOSFET,~~

having its source connected to second supply voltage, and having its gate connected to a source of accurate constant bias voltage.

9. (Currently amended) Capacitive feedback circuit according to claim [[7]] 8, wherein the second transistor has its drain connected to the source of the first transistor.

10. (Currently amended) Capacitive feedback circuit according to claim 2, wherein the current sensor comprises a combination of two transistors, ~~preferably MOSFETs,~~ connected in a current mirror configuration.

11. (Previously presented) Capacitive feedback circuit according to claim 7, wherein the current sensor comprises a third transistor having its source connected to first supply voltage and having its drain connected to the drain of the first transistor, and further comprises a fourth transistor having its source connected to first supply voltage and having its gate connected to the gate and to the drain of the third transistor.

12. (Currently amended) Capacitive feedback circuit according to claim [[2]] 4, wherein the comparator comprises a combination of two transistors, ~~preferably MOSFETs,~~ connected in a current mirror configuration.

13. (Previously presented) Capacitive feedback circuit according to claim 11, wherein the comparator comprises a fifth transistor having its source connected to second supply voltage and having its drain connected to the drain of the fourth transistor, and further comprises a sixth transistor having its source connected to second supply voltage and having its gate connected to the gate and to the drain of the fifth transistor.

14. (Original) Capacitive feedback circuit according to claim 13, wherein the comparator further comprises a reference current source coupled to provide a reference current to the drain of the sixth transistor, and wherein the drain of the sixth transistor is connected to said node.

15. (Original) Capacitive feedback circuit according to claim 14, wherein the reference current source a seventh transistor having its source connected to first supply voltage, having its drain connected to the drain of the sixth transistor, and having its gate connected to a source of accurate constant reference voltage.

16. (Currently amended) Voltage regulator comprising a capacitive feedback circuit according to claim [[1]] 2.

17. (Currently amended) Voltage regulator comprising:

a voltage input terminal;

a voltage output terminal;

an input differential amplifier, comprising a differential input stage which comprises:

a first series arrangement of a first transistor~~, preferably a MOSFET,~~ and a first current source;

a second series arrangement of a second transistor~~, preferably a MOSFET,~~ and a second current source;

and a non-linear resistor having a first terminal connected to a first node between the first transistor and the first current source and having a second terminal connected to a second node between the second transistor and the second current source;

said input differential amplifier having a signal input terminal connected to the regulator input terminal;

an output driver stage comprising:

a voltage input connected to an output of the input differential amplifier;

a voltage output;

a current feedback loop feeding back a signal representative of the output current provided at said voltage output such as to effectively decrease

the AC-impedance at said voltage input in order to increase the gain for AC signals;

voltage feedback means having an input connected to the regulator output terminal and having an output connected to a feedback input terminal of the input stage;

and a capacitive feedback circuit according to claim 1, having its input terminal connected to the regulator output terminal and having its output terminal connected to the input of the output driver stage;

wherein said voltage regulator further has one or more of the following features:

(a) the non-linear resistor comprises a third transistor, ~~preferably a MOSFET,~~ having its source connected said first node, having its drain connected to said second node, and having its gate connected to a constant bias voltage;

(b) the first current source is connected between a source of the first transistor and a voltage reference;

the second current source is connected between a source of the second transistor and said voltage reference;

and said three transistors mutually are of the same conductivity type;

(c) the output driver stage comprises:

an input transistor, ~~preferably a MOSFET,~~ having its source connected to a controllable impedance, and having its gate connected to the input terminal; wherein said controllable impedance ~~preferably~~ comprises:

two transistors, ~~preferably MOSFETS,~~ connected in current mirror configuration, wherein a first one of said transistors has its source connected to a first supply voltage level, and has its drain connected to a bias current source, and wherein a second one of said transistors has its source connected to a first supply voltage level, has its drain connected to the source of the input transistor, and has its gate connected to the gate and to the drain of the said first transistor;

an output transistor, ~~preferably a MOSFET,~~ having its source connected to a first supply voltage level, and having its drain connected to the output terminal;

current coupling means coupled between the drain of said input transistor and the gate of said output transistor; wherein said current coupling means ~~preferably~~ comprise:

two transistors, ~~preferably MOSFETS,~~ connected in current mirror configuration, wherein one transistor has its source connected to a second supply voltage level and has its drain connected to the drain of the input transistor, and wherein the other transistor has its source connected to said second supply voltage level, has its drain connected to a first bias current source and to the gate of said output transistor, and has its gate connected to the gate and to the drain of the said one transistor;

an output current sensor associated with the output transistor, providing a sensor output current signal representing the output current; wherein the output current sensor ~~preferably~~ comprises a sensor transistor of the same conductivity type as the output transistor, having its source and gate connected in parallel to the source and gate of the output transistor;

a current feedback loop feeding back a signal derived from the sensor output current signal to control said controllable impedance; wherein the current feedback loop ~~preferably~~ comprises:

two transistors, ~~preferably MOSFETS,~~ connected in current mirror configuration, wherein one transistor has its drain connected to receive said sensor output current signal and wherein the other transistor has its drain connected to the source of the input transistor.